Claims:

sub a4

1. A non-volatile memory package comprising:

a substrate having a first surface and a second surface;

an integrated circuit die including a memory array mounted to the first surface of the substrate; and

a passive component mounted to the second surface of the substate.

2. The non-volatile memory package of claim 1, wherein the passive component is electrically coupled to the integrated circuit die.

3. The non-volatile memory package of claim 1, further comprising an array of solder balls mounted to the substrate.

4. The non-volatile memory package of claim 3, wherein the passive component is located centrally within the array of solder balls.

5. The non-volatile memory package of claim 4, wherein the passive component has a height less than a height of the solder balls.

6. The non-volatile memory package of claim 1, wherein the passive component is at least a portion of a voltage regulator circuit coupled to the integrated circuit die.

7. The non-volatile memory package of claim 1, wherein the substrate comprises a cavity and at least a portion of the passive component lies within the cavity.

8. The non-volatile memory package of claim 7, further comprising an array of solder balls mounted to the substrate, wherein the passive component has a height less than a height of the solder balls.

9. The non-volatile memory package of claim 1, wherein the passive component is mounted to the substrate with an epoxy material.

10. The non-volatile memory package of claim 10, wherein the epoxy material between the passive component and the substrate is less than about 0.1 millimeters in thickness.

11. The non-volatile memory package of claim 1, wherein the passive component is mounted to the substrate with a conductive material.

12. The non-volatile memory package of claim 1, wherein the passive component includes a capacitor or an inductor.

13. The non-volatile memory package of claim 1, wherein the integrated circuit die includes a flash memory array.

14. 13. A method comprising:

forming a substrate;

mounting an integrated circuit die on said substrate;

mounting a passive component overly the substrate; and

electrically coupling the passive component to at least a portion of the integrated circuit die.

15. 14. The method of claim 13, further comprising adhesively attaching the passive component to the integrated circuit die.

16. 15. The method of claim 14, further comprising adhesively attaching the passive component to the integrated circuit die with a non-conductive adhesive.

17. 16. The method of claim 13 including wire bonding the passive component to the substrate.

18. 17. The method of claim 13 including wire bonding the passive component to the integrated circuit die.

19.
18. A method comprising:

molding an integrated circuit die and at least one passive component of a voltage regulator circuit into a package, the integrated circuit die including a non-volatile memory array.

20.
19. The method of claim 18, further comprising mounting the at least one passive component to the integrated circuit die.

21.
20. The method of claim 18, further comprising forming a wire bond to electrically couple the at least one passive component and the integrated circuit.